A LOW-POWER X-BAND FREQUENCY SYNTHESIZER MODULE

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ABSTRACT

This paper describes an X-band frequency synthesizer that features low power consumption. To save power and reduce cost, new MMIC's were developed and combined with commercially available components. With +10 dBm output, the power consumption is 270 mW, the lowest ever reported for X-band synthesizers.

INTRODUCTION

There is a growing demand for wireless communications at high data rates for multimedia services [1]. High data rates require more bandwidth and hence higher carrier frequency. Currently, wireless local area network (LAN) systems providing 10 Mbit/s in the 19-GHz band are available in Japan, and other systems with high data rates are being investigated worldwide [2], [3]. The next generation of wireless LAN's will use portable terminals and service coverage will be expanded to the outdoors [4], [5]. Because these terminals will be battery operated, power consumption must be minimized. Further reductions of power consumption have been difficult due to the use of local oscillators that consist of many analog and digital circuits. The power consumption of local oscillators, including fixed frequency oscillators, beyond the C-band is more than 1 W [6]-[13].

This paper presents an X-band frequency synthesizer whose power consumption is only 270 mW with +10 dBm output. To achieve the low power consumption and reduce cost, we developed new MMIC's and combined them with commercially available devices. All the elements are fabricated on a board.

SYNTHESIZER MODULE DESIGN

Our target frequency for the local oscillator is 9.6 GHz. The oscillator is combined with a harmonic mixer for 19 GHz frequency conversion. There are several configurations with which 9.6 GHz output can be obtained, among them 9.6 GHz direct oscillation and 9.6/n GHz oscillation with times-n multiplication, where n is an integer. Direct oscillation at 9.6 GHz can be effortlessly obtained with a mature GaAs MESFET process; however, frequency dividers following a voltage-controlled oscillator (VCO) have more than 400 mW dissipation [14], [15]. On the other hand, larger n results in spurious signal increase around the carrier.

A configuration with 2.4-GHz oscillation and times-4 multiplication was selected to meet power, cost and performance requirements. In the 2.4-GHz band, devices using a 3 V supply are commercially available for the VCO and the phase-locked loop (PLL) IC. Many types of VCO's have been developed with the ongoing development of new types of MMIC's; however, they typically have rather high phase noise. A hybrid configuration for the VCO may well be an effective means of addressing this problem. The multipliers and amplifiers, in contrast, are MMIC's designed for low-power performance.

Figure 1 shows a block diagram of the X-band frequency synthesizer along with its level diagram. Level design affects power consumption directly. Saturation output power is proportional to DC power dissipation. Accordingly, all signal levels except that at the final stage are set low, or in other words, the allowable current dissipation is low. Final output power meets the system requirement, which is more than +8 dBm.

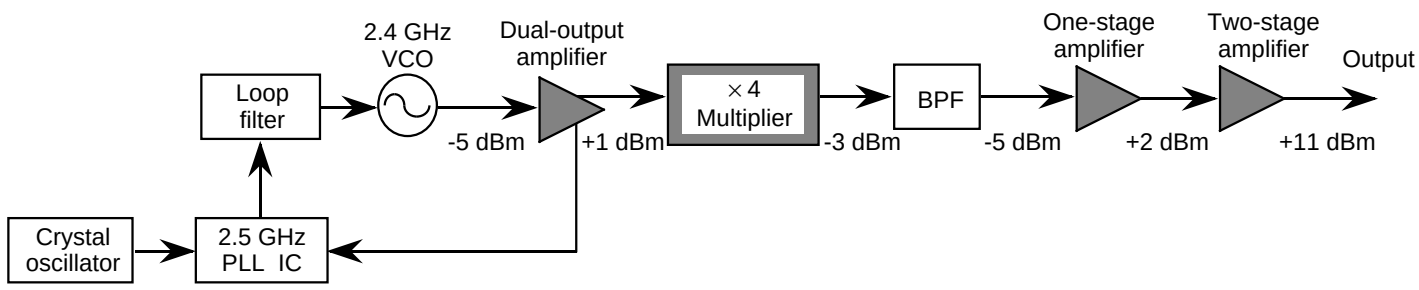

Figure 1: Module configuration and its level diagram.

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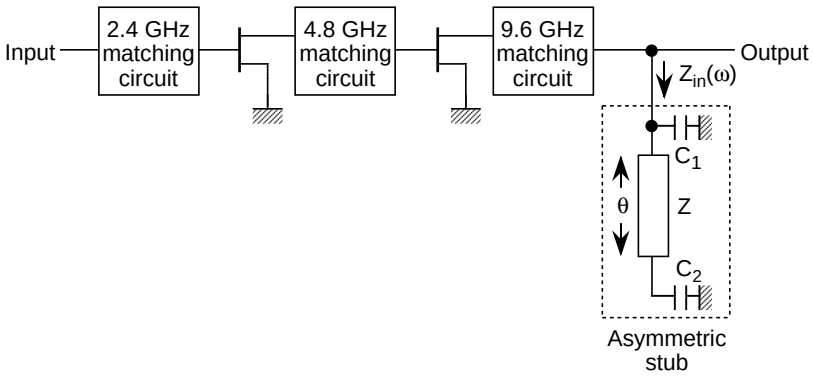

Figure 2: Frequency quadruplier with an asymmetric stub.

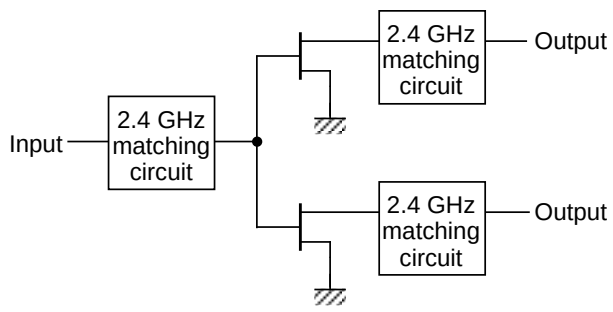

Figure 3: Dual-output amplifier.

MMIC DESIGN AND PERFORMANCE

Multiplier

Commercially available microwave frequency doublers are usually diode type, thus their DC power dissipation is 0. However, their conversion loss is generally more than 10 dB, and hence more than 20 dB for frequency quadrupliers, i.e., two-stage doublers. Moreover, the required input power is more than +10 dBm. The power consumption of amplifiers for driving the frequency doubler and compensating conversion loss is therefore large.

FET multipliers biased in the nonlinear operation region have low conversion loss and low input power [16]. However, they pose a problem for fundamental frequency suppression. Though a balanced configuration is attractive for fundamental frequency suppression [17], this type of FET multiplier dissipates twice as much power as a single FET multiplier. A single-ended FET multiplier combined with a quarter wavelengh stub can suppress the fundamental frequency component. However, the stub is quite large at the 4.8 GHz band, i.e., 6.3 mm on a GaAs substrate. This results in high chip cost. A quarter-wavelengh transmission line can be shortened by combining a high impedance transmission line with shunt capacitors [18]. Unfortunately, the open frequency of the shortened transmission line is not a harmonic of the short frequency, thus it is not suitable for the stub of the multipliers.

We devised an asymmetric stub and applied the single-ended FET multiplier shown in Fig. 2. Capacitors C_1 and C_2 are

$$C_1 = \frac{1}{\omega_o Z \tan\theta} \quad (1)$$

$$C_2 = \frac{C_1 \cos^2\theta}{2\cos^2\theta + 1} \quad (2)$$

where ω_o, Z, θ are the fundamental angular frequency, the characteristic impedance of the stub, and the electrical angle of the stub, respectively. When frequency ω is equal to ω_o, the input impedance of the stub, $Z_{in}(\omega)$, is 0. When ω is equal to $2\omega_o$, $Z_{in}(\omega)$ is ∞.

This stub was fabricated by using equivalent lumped elements and applied to a 2.4 to 9.6 GHz frequency quadruplier MMIC with single-ended configuration, where the fundamental frequency of the stub, f_o, is 4.8 GHz. The resulting GaAs chip area is 1.5 mm × 1.5 mm. The 2.4-GHz frequency component is suppressed at the 9.6 GHz matching circuit. Matching circuits were determined on the basis of a harmonic-balance analysis to obtain low conversion loss when input power is 0 dBm. Measured conversion loss is 4.2 dB and the power consumption is 39 mW (3 V • 13 mA) with 2.4 GHz-0 dBm input.

Dual-output amplifier

The VCO output should be split in two with isolation to prevent the noise of the PLL digital circuit from mixing with the RF signal. Hybrid couplers such as the Wilkinson divider do not have the isolation out of their bandwidth and the circuit is large. A resistive power splitter combined with an attenuator is attractive; however, the amplifiers use a lot of power in compensating for resistive loss. We adopted the dual-output amplifier shown in Fig. 3 to achieve wideband isolation and reduce power and chip area. The gates of two FET's are connected and follow the input matching circuit. Output signals have isolation owing to the reverse transmission coefficient, S12, of the FET.

The dual-output amplifier is integrated on a 1.5 mm × 1.5 mm GaAs chip. Measured gain is 6.3 dB and isolation between the two outputs is 22 dB at 2.4 GHz. The power consumption is 54 mW (3 V • 18 mA).

X-band amplifier

The one-stage amplifier consists of 100 μm FET and is integrated on a 1.5 mm × 1.5 mm GaAs chip. Measured gain is 8.0 dB at 9.6 GHz. The power consumption is 30 mW (3 V • 10 mA).

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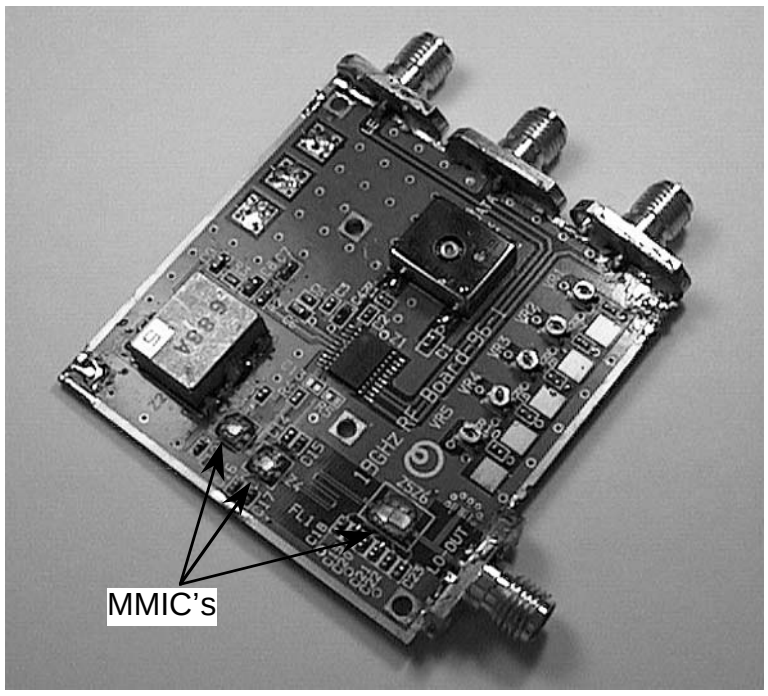

Figure 4: Frequency synthesizer module.

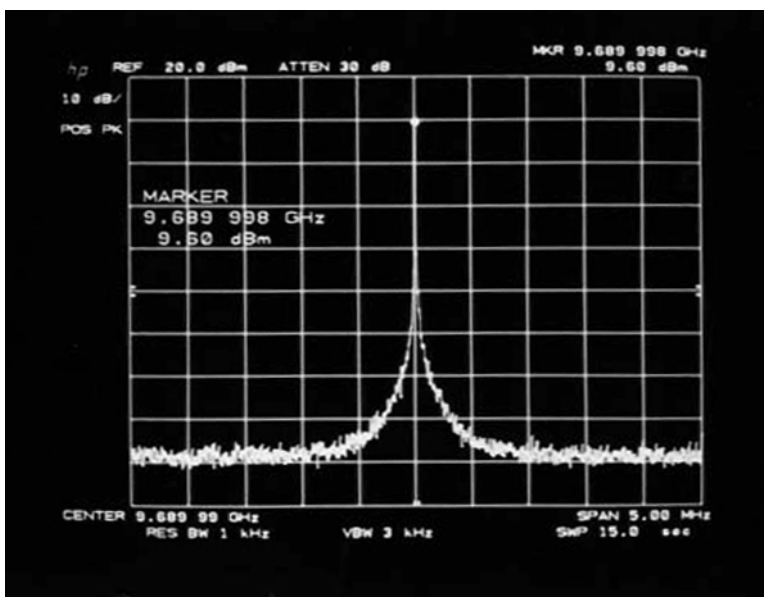

Figure 5: Synthesizer module output spectrum.
H: 500 kHz/div; V: 10 dB/div; R: 1 kHz.

The two-stage amplifier consists of a 100 μm FET for the first stage and a 200 μm FET for the second stage. It is integrated on a 2.0 mm × 1.5 mm GaAs chip. Measured gain is 14.3 dB at 9.6 GHz. The power consumption is 90 mW (3 V • 30 mA).

SYNTHESIZER MODULE PERFORMANCE

All the circuits are implemented on a board as shown in Fig. 4, where MMIC bare chips are mounted on the board and coated with silicone rubber. The module is 50 mm × 50 mm × 6 mm and the weight, excluding the connectors, is 8 g. The board material is BT resin [19]. The loss tangent, tanδ, of the BT resin in the module is 0.0038 and its relative dielectric constant, ε_r, is 3.3 at 10 GHz.

A bandpass filter follows the frequency quadruplier and it

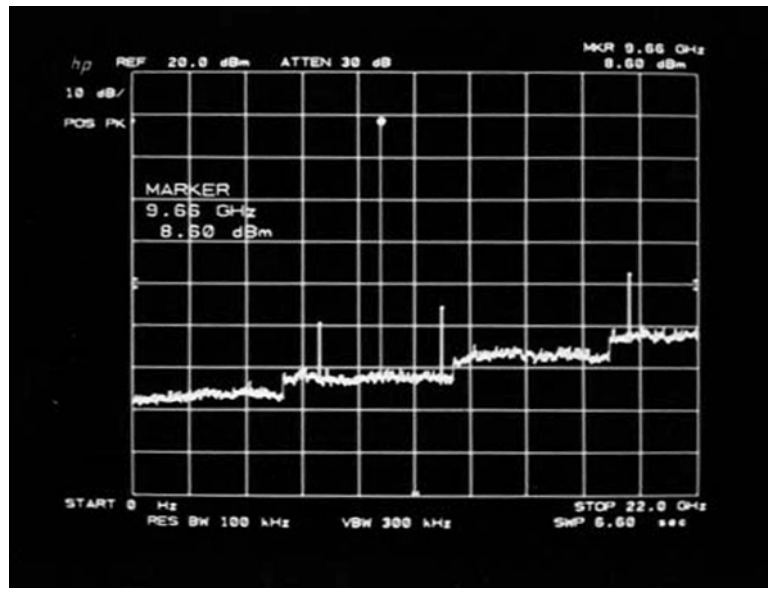

Figure 6: Wide span spectrum.
H: DC-22 GHz; V: 10 dB/div; R: 100 kHz.

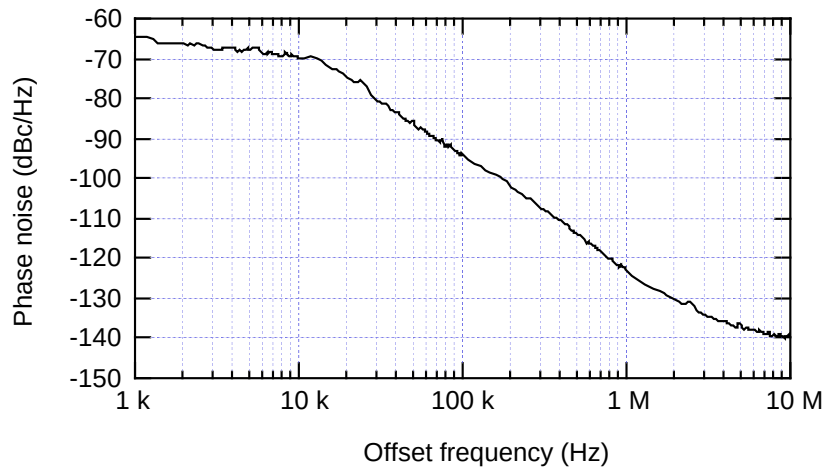

Figure 7: Phase noise performance.

was formed on the board with cascaded coupled lines. It has a measured insertion loss of 1.7 dB at 9.6 GHz, 23.3 dB at 9.6-2.4 = 7.2 GHz, 26.2 dB at 9.6+2.4 = 12 GHz.

Output spectrum is shown in Fig. 5. Loss of the cable used in the measurement was 0.55 dB. The output power of the module is therefore +10.15 dBm. Figure 6 is the DC-22 GHz span spectrum. Spurious levels at the nearest carrier, 9.6 ± 2.4 GHz, are at least 43 dB below the carrier. Phase noise performance is shown in Fig. 7 when the frequency step size is 10 MHz at 9.7 GHz. Phase noise at 1-MHz offset from the carrier is -123 dBc/Hz.

The current dissipations of the VCO, the PLL IC, and the crystal oscillator used in the synthesizer module are 6.5, 11, and 1.5 mA under +3 V supply. The total power consumption of the frequency synthesizer module is 270 mW (3 V • 90 mA). The power consumption, the output frequency, and the output power (dBm) of the PLL oscillators are compared in Fig. 8. To the author's knowledge, this power consumption is the lowest ever

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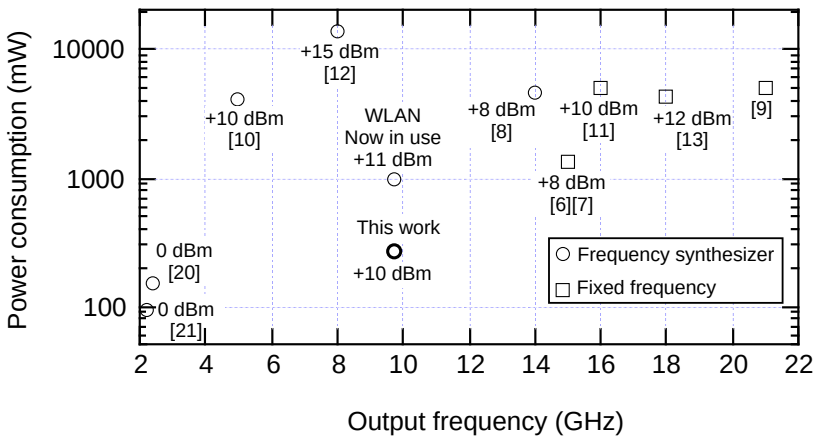

Figure 8: PLL oscillator comparison.

reported for X-band frequency synthesizers with +10 dBm output.

CONCLUSION

A new X-band frequency synthesizer module has been developed that features low power consumption. To achieve the low power consumption and reduce cost, MMIC's of a frequency quadruplier with an asymmetric stub, a dual-output amplifier, and X-band amplifiers were newly developed after the module configuration selection and level diagram design, and were combined with a commercially available VCO, PLL IC, and crystal oscillator. The total power consumption of the frequency synthesizer module is 270 mW with +10 dBm output, which is the lowest ever reported for X-band frequency synthesizers. This module can be applied to wireless personal communications with high data rates.

ACKNOWLEDGMENT

The authors would like to thank Dr. M. Muraguchi and M. Nakatsugawa for their helpful discussions, F. Saito for assistance in module assembly. They also wish to thank A. Hashimoto for his advice and encouragement.

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